SMWD 2023, KTH Royal Institute of Technology, Stockholm, 23$^{rd} - 25^{th}$May2023

Characterisation of resonant tunnelling diodes up to 1100 GHz

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Summary

This paper presents the ongoing development of resonant tunnelling diodes and on-wafer characterisation up to 1100 GHz. Utilising multiline-TRL and de-embedding structures, the S-parameters of the diodes will be measured, and the intrinsic device parameters extracted. The resonant tunnelling diodes are fabricated on a semi-insulating InP wafer as a double-barrier structure of $In_{0.53}Ga_{0.47}As/AlAs$.

1 Introduction

Owing to the characteristics of electromagnetic waves, the terahertz spectrum, stretching from 300 GHz to 10 THz, has shown promise for several applications, such as environmental and biomedical analysis and communications. Estimations based on the atmospheric attenuation indicate that 1.5 THz of suitable spectrum for short-range point-to-point links using 50 GHz bands, between 300 GHz and 2 THz alone. Efficiently utilising this spectrum requires effective fundamental sources. Owing to their simple designs and capability of room temperature operation, the resonant tunnelling diodes (RTD) show potential. Recent work demonstrates that the RTD is capable of fundamental oscillations up to 1.98 THz [1] and has comparable output power results to other sources [2]. However, to achieve the full potential of the RTDs, there is a need for on-wafer characterisation and modelling. Previous works have developed it for frequencies up to 110 [3] and 500 GHz, and we will extend it to 1100 GHz with this work.

2 Fabrication

The samples are fabricated in the Nanofabrication laboratory at the Chalmers University of Technology. A schematic process flow for the RTDs is shown in Figure 1, and the steps are as follows. The epitaxial structure is initially grown using molecular beam epitaxy on the semi-insulating InP wafer. After which the collector contact, consisting of Ti/Au/Pd/Ti, where the top titanium layer serves as an etch mask for the next step, is deposited using a lift-off technique. Then dry etching using inductively coupled plasma defines the active RTD mesa. Using the same lift-off technique, the emitter contact in Au/Pd/Ti is deposited next; however, annealing is subsequently performed to improve the ohmic contact of the emitter and collector. Afterwards, the finished devices are isolated by wet etching using $H_3PO_4 : H_2O_2 : H_2O$ (1:1:38). This solution has a high selectivity towards InP and an etch rate of approximately 100 nm per minute, allowing for a complete etch to the substrate and low risk of over-etching the device. The final steps are to fabricate coplanar waveguides (CPW) in Au/Ti and contact them to the device, where the signal path to collector contact has an air-bridge structure.

3 Characterisation

Characterisation of the RTDs will be done through S-parameter measurements. The measurements will be performed on-chip using VNA, frequency extenders and T-wave probes with biasing capabilities. The on-chip probe pads will be connected to the RTDs through 50 Ohm CPW. A multiline-TRL [5] calibration standard using four lines located on-chip will shift the reference plane to the device. De-embedding of the contacting structures will be used to extract the S-parameters at the intrinsic device. The data from several S-parameter measurements at different quiescent points will be used to extract the device parameters according to an RTD small signal model.

4 Acknowledgements

The authors thank Vladimir Drakinskiy for providing his expertise and advice on fabrication techniques and tools. The work presented in this paper is supported by the Swedish Foundation for strategic research (SSF), project number CHI19-0027.

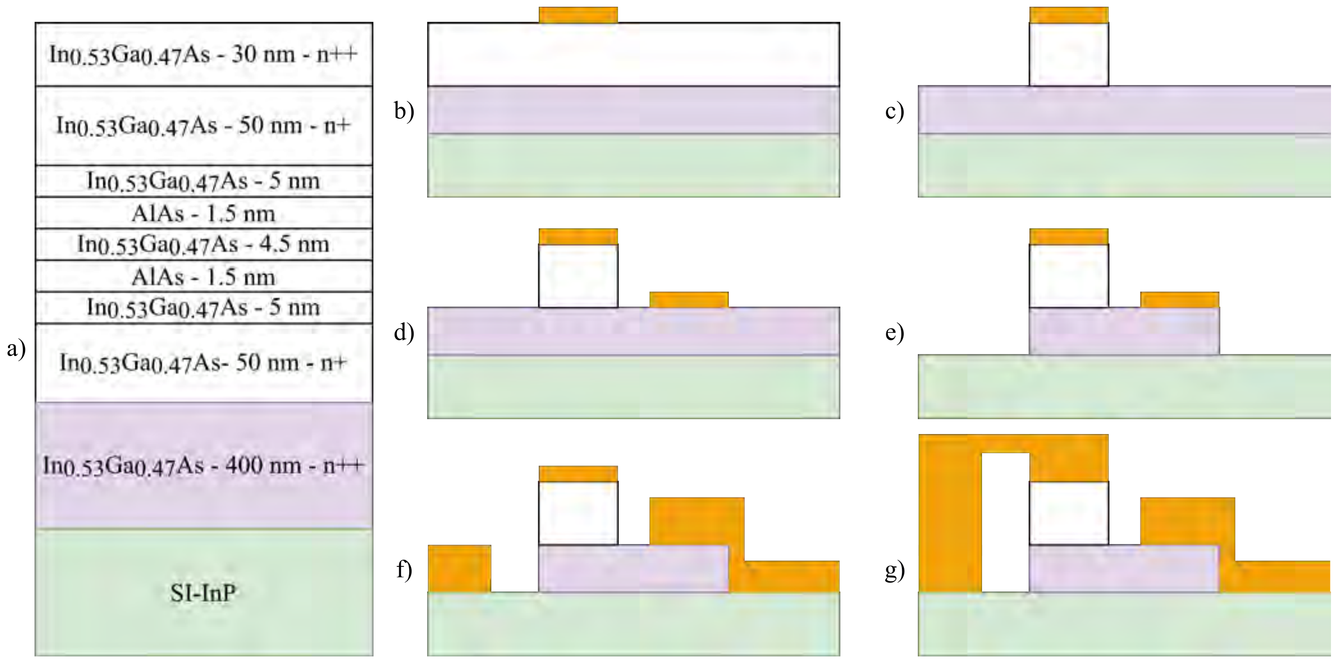

Figure 1. Fabrication process flow. a) Epitaxial structure. b) Collector contact deposition. c) RTD mesa defined. d) Emitter contact deposition. e) Device isolation. f), g) CPW and contact deposition.

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